IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A system LSI being formed on one chip, comprising:

a storage circuit in which at least one program has been stored;

at least one processor circuit for carrying out a processing operation in accordance with said program, said processor circuit having a program counter, at least one computing unit and at least one register; ~~and~~

a peripheral circuit, capable of sending and receiving a signal to and from said processor circuit, for carrying out a predetermined logical operation in accordance with an input signal, said peripheral circuit having at least one functional block[[,]] ; and

said system LSI further comprising[[:]] selection means for optionally selecting one ~~of the outputs~~ output of said program counter, said computing unit and said register in said processor circuit, at least one output of said storage circuit, and one ~~of the outputs~~ output of a plurality of internal signals in said peripheral circuit including ~~the~~ an output of said functional block[[;]], and

selection control means for controlling selection of a result signal from any operation process in any place of said processor circuit, said storage circuit and said peripheral circuit, on the basis of a selection signal which is supplied from ~~the~~ an outside of said system LSI via an external terminal.

Claim 2 (Original): A system LSI as set forth in claim 1, wherein said processor circuit further comprises a debug backup circuit having an internal control signal generating portion for generating an internal control signal during a processing operation, and said selection means carries out a selecting operation on the basis of said internal control signal,

which is generated by said internal control signal generating portion of said processor circuit, and said selection signal which is supplied from the outside.

Claim 3 (Original): A system LSI as set forth in claim 1, wherein said selection means comprises:

a first selection circuit, provided in said processor circuit, for optionally selecting and outputting at least one value of said program counter, said computing unit, said register and said storage circuit;

a second selection circuit, provided in said peripheral circuit, for optionally selecting and outputting one of a plurality of internal signals in said peripheral circuit, which include the output of said functional block; and

a third selection circuit for optionally selecting one of the outputs of said first and second selection circuits to output the selected one to the outside.

Claim 4 (Original): A system LSI as set forth in claim 3, wherein said processor circuit further comprises a debug backup circuit having an internal control signal generating portion for generating an internal control signal during a processing operation, and said first through third selection circuits carry out a selecting operation on the basis of said internal control signal, which is generated by said internal control signal generating portion of said processor circuit, and said selection signal which is supplied from the outside.

Claim 5 (Currently Amended): A system LSI as set forth in claim 3, which further comprises a plurality of processor circuits, each of which is said processor circuit according to claim 3, and

wherein said second selection circuit carries out a selecting operation on the basis of a control signal which is generated while each of said plurality of processor circuits is operating, and

said third selection circuit optionally selects one of the output of said first selection means and the output of said second selection means on the basis of a control signal, which is ~~generates~~ generated while each of said plurality of processor ~~circuit~~ circuits is operating, and a control signal which is supplied from the outside, to output the selected output to the outside.

Claim 6 (Original): A system LSI as set forth in claim 5, wherein each of said plurality of processor circuits comprises a debug backup circuit having an internal control signal generating portion for generating an internal control signal during a processing operation, and said first through third selection circuits carry out a selecting operation on the basis of said internal control signal, which is generated by said internal control signal generating portion of each of said plurality of processor circuits, and said selection signal which is supplied from the outside.

Claim 7 (Original): A system LSI as set forth in claim 5, wherein at least one of said first, second and third selection circuits has a serial/parallel converter circuit for serial/parallel converting a selected signal to output the converted signal to the outside of said LSI.

Claim 8 (Original): A system LSI as set forth in claim 5, wherein at least one of said first, second and third selection circuits has a parallel/serial converter circuit for

parallel/serial converting a selected signal to output the converted signal to the outside of said LSI.

Claim 9 (Original): A system LSI as set forth in claim 5, wherein at least one of said first, second and third selection circuits has a thinning-out circuit for thinning out selected signals at regular intervals to output the thinned-out signals to the outside of said LSI.

Claim 10 (Original): A system LSI as set forth in claim 1, wherein said LSI has a plurality of input/output terminals for sending and receiving signals to and from a system LSI peripheral device.

Claim 11 (Original): A system LSI as set forth in claim 10, wherein any one of said plurality of input/output terminals is used for inputting/outputting a monitor control signal for debug and a monitor signal.

Claim 12 (Original): A system LSI as set forth in claim 1, wherein said LSI further comprises an input terminal only for inputting a monitor control signal for debug, and an output terminal only for outputting the monitor signal after monitoring.

IN THE DRAWINGS

The attached sheet of drawings includes changes to Fig. 6. This sheet, which includes Fig. 6, replaces the original sheet including Fig. 6.

Attachment: Replacement Sheet (1)